

# ACKNOWLEDGEMENT RECEIPT

Electronic Version

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**Title of  
Invention**

**STRUCTURE AND METHOD OF MAKING STRAINED  
SEMICONDUCTOR CMOS TRANSISTORS HAVING  
LATTICE-MISMATCHED SOURCE AND DRAIN REGIONS**

Submission Type :

Utility Patent Filing

Application Number:

10/604607



EFS ID:

44758

Server Response:

Confirmation Code	Message
ISVR1	Submission was successfully submitted - Even if Informational or Warning Messages appear below, please do not resubmit this application
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First Named Applicant:

Huajie Chen

Attorney Docket Number:

FIS920030199US1

Timestamp:

2003-08-04 15:07:41 EDT

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US

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us-assignment	FIS920030199US1Assignment212.tif	18489	2003-08-04
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application-body	soamsb.ent	3988	2003-08-04
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